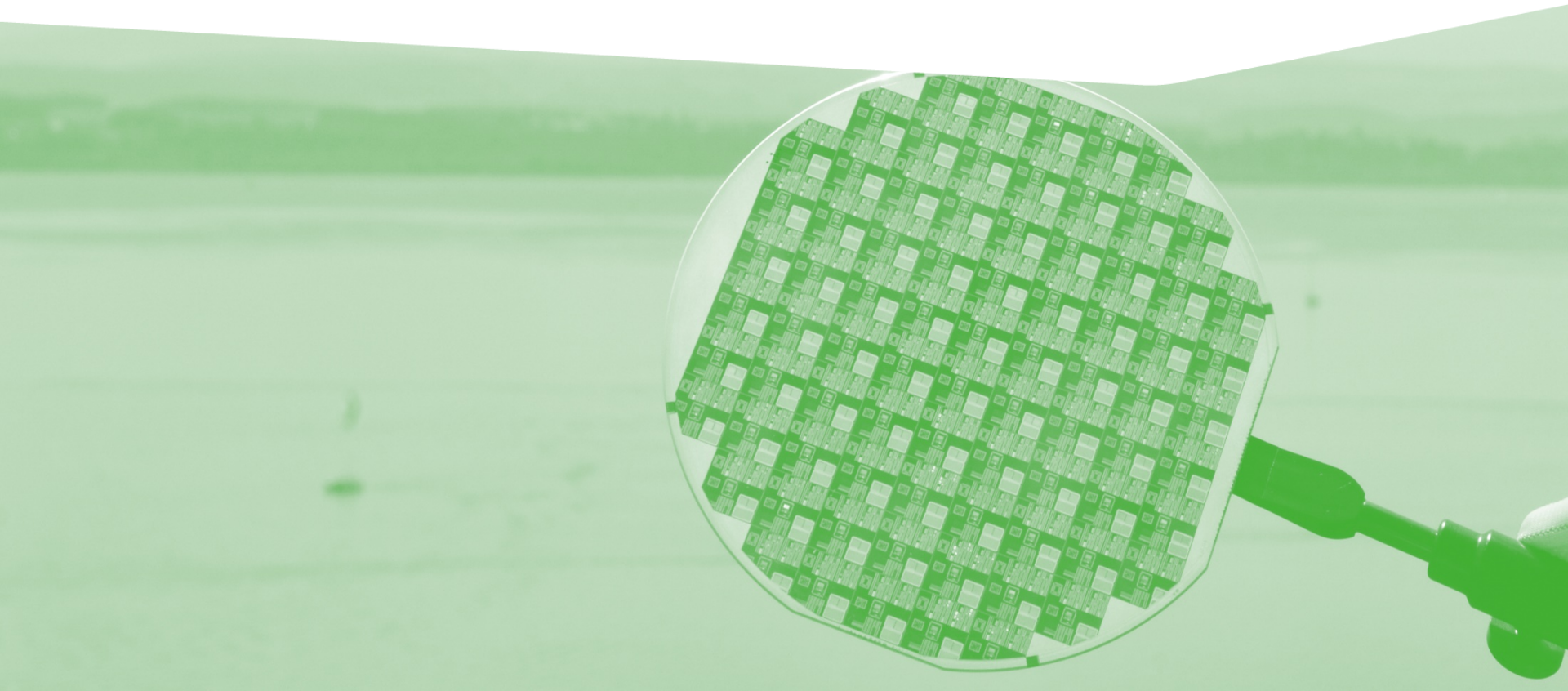
aptasic

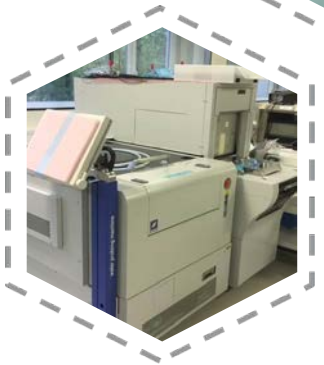
MUCH MORE THAN ASIC TEST

ATE AND CMOS IMAGERS



EQUIPMENT

ATE AND PROBERS dedicated to CMOS imager probing



LTXC D10 ATE mixed signal

D10 configuration: (2x) DPIN96,VIS16,DPS, MultiWave, DIBU

EG4090 Prober

8 inches prober (Dark & clean set-up)

Ex3000 Accretec prober

12 inches prober (Dark light and clean set-up)

From “standard” to custom solutions

Test Solution = HW + SW specific development

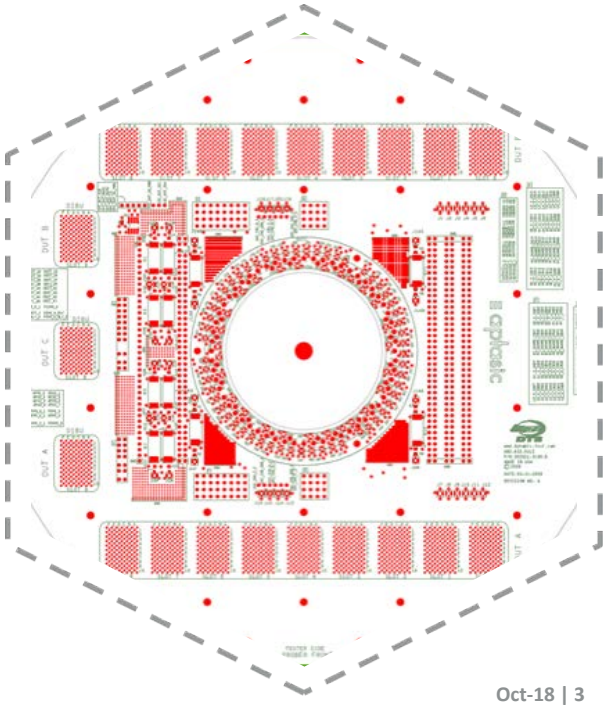
Standard HW development by Aptasic :

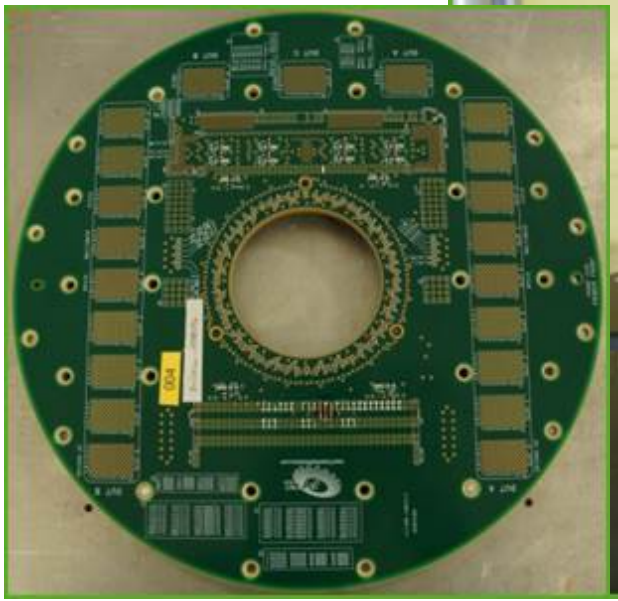
Standard Load-Board 84 signals

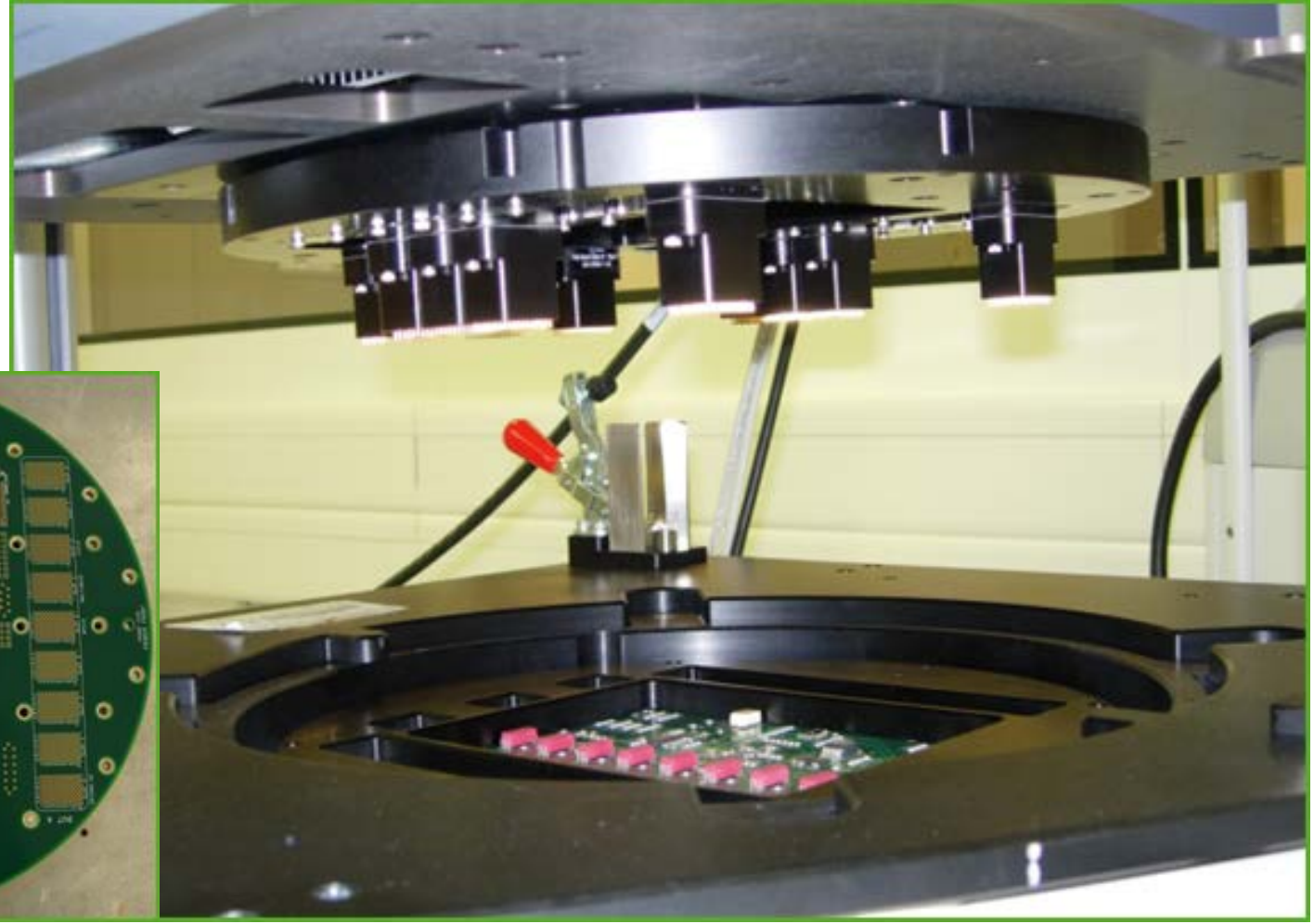
SW developed by Aptasic:

High level language code (C/C++)

Low investment - short lead time for first tested Silicon







From “standard” to custom solutions

84 pin HW ProbeCard

Compatible with former concept

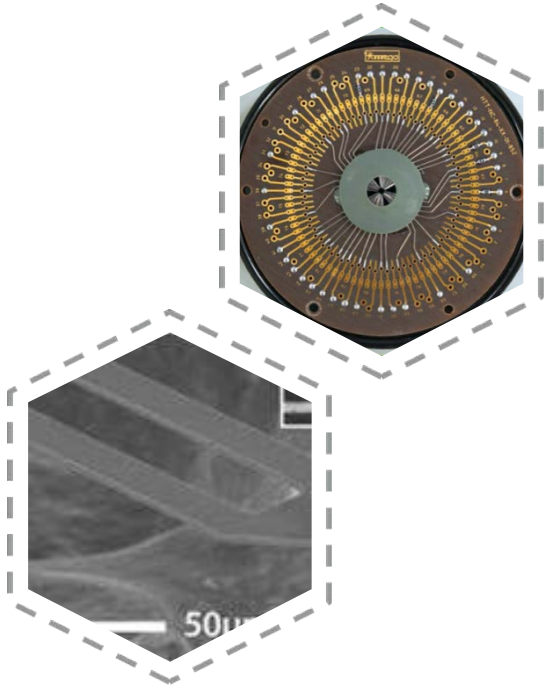
Used for wafer probing

- One needle to contact each pad or solder bump (WLCSP)

Spider with cantilever or vertical needles to ensure precise position of each needle

Fixed on the main Load-Board

Project specific



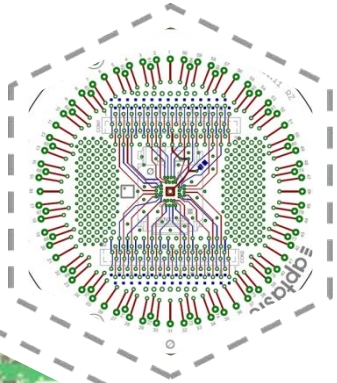
From “standard” to custom solutions

84 pin HW DUT-board

Compatible with Loadboard concept
Used for manual test

ZIF socket soldered on it to ensures contact with DUT
Flat cable connectors

Fixed on the main LoadBoard



From “standard” to custom solutions

Dedicated Handler Board

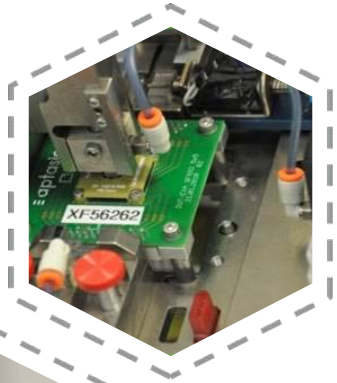
Automatic DUT contact block

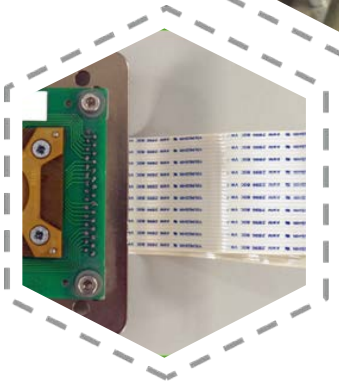
PCB contains the footprint for the test socket

Interfaces with the handler robot

Precise position on the handler

Project specific





CMOS IMAGERS TEST CONCEPT

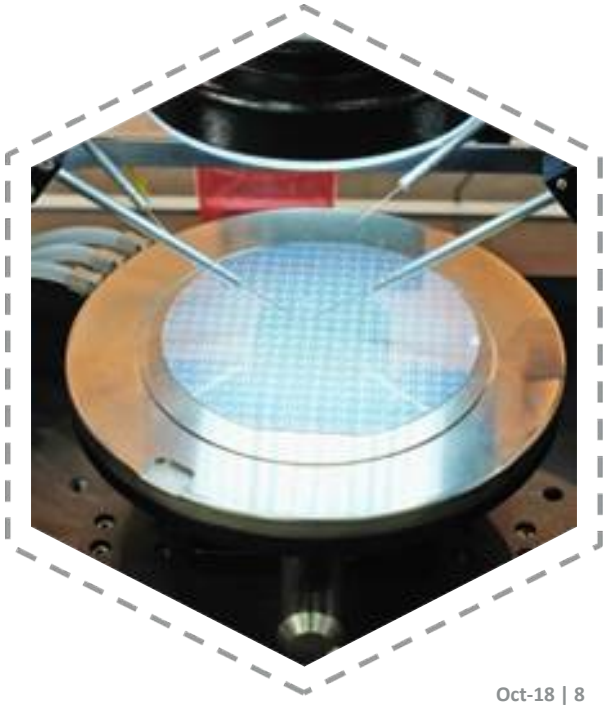
Layout

Test flow

- **Structural tests**
- **Functional tests**
- **Performance tests**

HW interfaces

- **Load-board** (Test Adapter Interface for imagers)
- **Probe-Card** (wafer test)
- **Light source** (variable light flow)



CMOS IMAGERS ILLUMINATION INTEGRATION

Custom illumination integrated to Loadboard

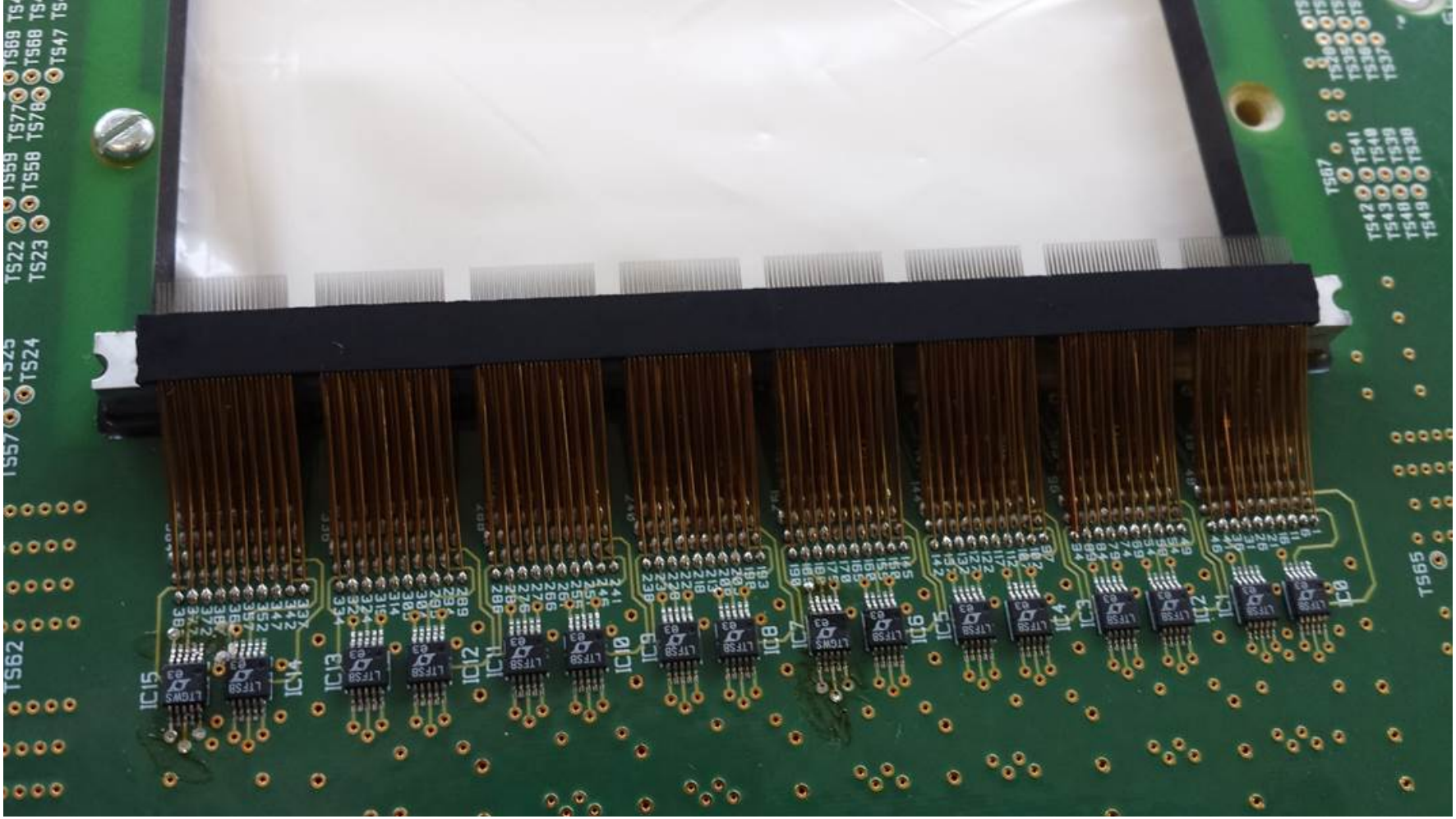
Light Source Specifications and calibration

Intensity and Wavelength Control

Uniformity (Noise reduction)

Large spectrum

Diffuser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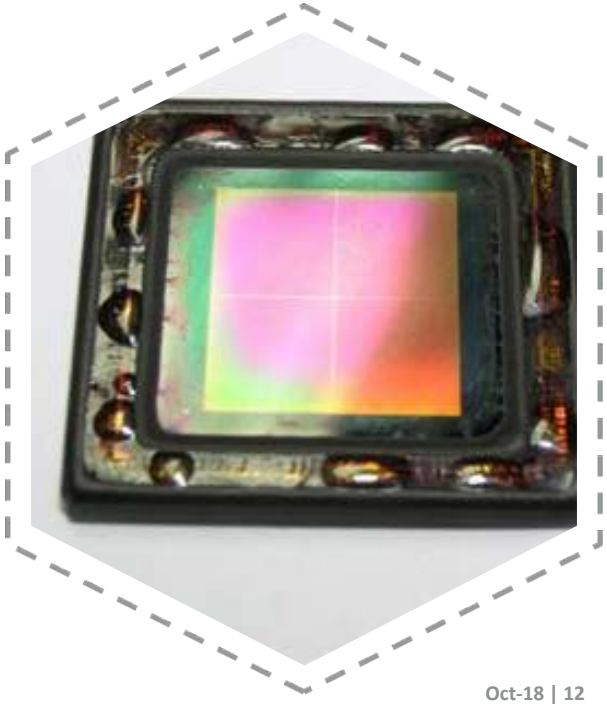
CMOS IMAGERS STRUCURAL / FUNCTIONNAL TEST

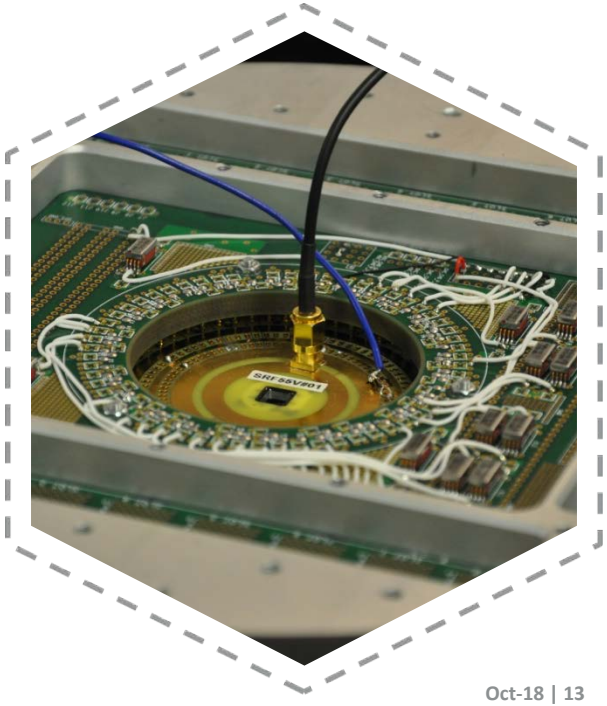
Test descriptions

1. Signal pad Opens-and-shorts and leakage current tests
2. Basic power draw at hardcoded defaults
3. Serial control register (SPI port) test
4. DACs test
5. Digital control signals test
6. Power shorts on array columns test
7. Test pixels test
8. Power draw vs. IBias DAC settings
9. Functional evaluation
   - Video Amp gain selection and column binning
   - S/H time constant selection
   - Dynamic gain switching
   - Pixel gain selection functionality
   - Row binning



CMOS IMAGERS PERFORMANCE EVALUATION

10. Performance evaluation
    - Pixels offset and electronic noise
    - Pixels leakage current
    - Video buffer electronic noise
    - Sensitivity, Saturation levels and saturation artifacts
    - Linearity
    - Video amplifier settling
    - Crosstalk, non-uniformity and other image artifacts over signal range and steps in image
11. Defective pixels, row segments, column segments, rows, columns
    - Test results reporting
    - Default acquisition timing sequence
    - Correlated double sampling



Take away

- Structural and performance test on Wafer and package verification
- Hardware concept easy to deploy
- Test flow tailored to your coverage requirement

… up to 12 inches Wafers!

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MUCH MORE THAN ASIC TEST

THANKS FOR YOUR ATTENTION